DEFENSE MICROELECTRONICS ACTIVITY (DMEA)
SMALL BUSINESS INNOVATION RESEARCH (SBIR) PROGRAM
SBIR FY07.2 Proposal Submission Instructions

INTRODUCTION

The DMEA SBIR program is implemented, administrated, and managed by the DMEA Program Control Division. If you have any questions regarding the administration of the DMEA SBIR program please contact the DMEA SBIR Program Manager (PM), Mr. Gene Graham, graham@dmea.osd.mil.

For general inquiries or problems with electronic submission, contact the DoD Help Desk at 1-866-724-7457 (1-866-SBIRHLP) (8am to 5pm EST). For questions about the topic during the pre-solicitation period (12 April 2007 13 May 2007) contact the Topic Authors listed under each topic on the http://www.dodsbir.net website prior to the solicitation. Information regarding the DMEA mission and programs can be found at http://www.dmea.osd.mil.

As funding is limited, DMEA will select and fund only those proposals considered to be superior in overall technical quality and most critical. DMEA may fund more than one proposal in a specific topic area if the technical quality of the proposal is deemed superior, or it may fund no proposals in a topic area.

PHASE I GUIDLEINES

DMEA intends for Phase I to be only and examination of the merit of the concept or technology that still involves technical risk, with a cost not exceeding $100,000.

A list of the topics currently eligible for proposal submission is included in this section followed by full topic descriptions. These are the only topics for which proposals will be accepted at this time. The topics are directly linked to DMEA's core research and development requirements.

Please assure that your e-mail address listed in your proposal is current and accurate. DMEA cannot be responsible for notification to companies that change their mailing address, their e-mail address, or company official after proposal submission.

PHASE I PROPOSAL SUBMISSION

Read the DoD front section of this solicitation for detailed instructions on proposal format and program requirements. When you prepare you proposal submission, keep in mind that Phase I should address the feasibility of a solution to the topic. Only UNCLASSIFIED proposals will be entertained. DMEA accepts Phase I proposals not exceeding $100,000. The technical period of performance for the Phase I should be 6 months. DMEA will evaluate and select Phase I proposals using review criteria based upon the technical merit and other criteria as discussed in this solicitation document. Due to limited funding, DMEA reserves the right to limit awards under any topic and only proposals considered to be of superior quality will be funded.

If you plan to employ NON-U.S. citizens in the performance of a DMEA SBIR contract, please identify these individuals in you proposal as specified in Section 3.5.b(7) of the program solicitation.

It is mandatory that the ENTIRE Technical Proposal, DoD Proposal Cover Sheet, Cost Proposal, and the Company Commercialization Report are submitted electronically through the DoD SBIR website at http://www.dodsbir.net/submission. If you have any questions or problems with the electronic proposal submission contact the DoD SBIR Helpdesk at 1-866-724-7457.

This COMPLETE electronic proposal submission includes the submission of the Cover Sheets, Cost Proposal, Company Commercialization Report, the ENTIRE Technical Proposal and any appendices via the DoD Submission site. The DoD proposal submission site http://www.dodsbir.net/submission will lead you through the process for submitting your technical proposal and all of the section electronically. Each of these documents is submitted

separately through the website. Your proposal submission must be submitted vial the submission site on or before the 6am 13 June 2007 deadline. Proposal submissions received after the closing date will not be processed.

PHASE II GUIDELINES

This solicitation solicits Phase I proposals. DMEA makes no commitments to any offeror for the invitation of a Phase II Proposal. Phase II is the prototype/demonstration of the technology that was found feasible in Phase I. Only those successful Phase I efforts that are INVITED to submit a Phase II proposal or Fast Track will be eligible to submit a Phase II proposal. DMEA does encourage, but does not require, partnership and outside investment as part of discussions with DMEA sponsors for potential Phase II invitation.

Invitations to submit a Phase II proposal will be made by the DMEA SBIR Program Manager (PM) in accordance with the process outlined below. Phase II proposals may be submitted for an amount normally not to exceed $750,000. DMEA will consider making Phase II Invitations with a base program of $750,000 and options. The base Program and options, together, may total a maximum of $2,500,000. FastTrack will be for $750,000 maximum, unless specified by the DMEA SBIR PM.

PHASE II PROPOSAL INVITATION

The DMEA topic manager and topic author will begin the process for a Phase II invitation by reviewing the Phase I work of each contractor, and will make a recommendation on what Phase I efforts should continue into Phase II. The DMEA recommendation is based on several criteria, including the Phase II Prototype/Demonstration (*What is being offered at the end of Phase II?*), Phase II Partnership (*Who are the partners and what are their commitment? Funding? Facilities? Etc.? This can also include Phase III partners*), and the potential Phase II cost.

The DMEA PM recommends the Phase II invitation, based on the above criteria and funding availability, to the DMEA Chief of Program Control. The DMEA Chief of Program Control has final approval authority. If approved, Phase II invitation is issued by the DMEA SBIR PM.

PHASE II PROPOSAL SUMMISSION

If you have been invited to submit a Phase II proposal, please contact the DMEA SBIR PM for further instructions.

All Phase II proposals must have a complete electronic submission. Complete electronic submission includes the submission of cover sheets, cost proposal, company commercialization report, the entire technical proposal, and any appendices vial the DoD submission site (http://www.dodsbir.net/submission). The DoD proposal submission site will lead you through the process for submitting your technical proposal and all of the sections electronically. Each of these documents are submitted separately through the website. Your proposal must be submitted via the submission site on ore before the DMEA-specified deadline or may be declined.

DMEA FAST TRACK DATES AND REQUIREMENTS

The complete Fast Track application must be received by DMEA 120 days from the Phase I award start date. The Phase II proposal must be submitted within 180 days of the Phase I award start date. Any FastTrack applications or proposals not meeting these dates may be declined. All Fast Track applications and required information must have a complete electronic submission. The DoD proposal submission site http://www.dodsbir.net/submission will lead you through the process of submitting your technical proposal and all of the sections electronically. Each of these documents is submitted separately through the website. Your proposal must be submitted via the submission site on or before the DMEA-specified deadline or may be declined.

The information required by DMEA is the same as the information required under the DoD Fast Track described in the front part of this solicitation. Phase I interim funding is not guaranteed. If awarded, it is expected that interim funding will generally not exceed $30,000. Selection and award of a Fast Track proposal is not mandated and DMEA retains the discretion not to select or fund any Fast Track proposal.

DMEA SBIR PHASE II ENHANCEMENT PROGRAM

To encourage transition of SBIR into DoD systems, DMEA has a Phase II Enhancement policy. DMEA's Phase II Enhancement program requirements include: up tot one year extension of existing Phase II, and up to $500,000 matching SBIR funds. Applications are subject to review of the statement of work, the transition plan, and the availability of funding. DMEA will generally provide the additional Phase I Enhancement funds by modifying the Phase II contract.

PHASE I PROPOSAL SUBMISSION CHECKLIST:

All of the following criteria must be met or your proposal will be REJECTED.

_____1. Your Technical Proposal, the DoD Cover Sheet, the DoD Company Commercialization Report (required even if your firm has no prior SBIRs), and the Cost Proposal have been submitted electronically through the DoD submission site by 6 a.m. EST 13 June 2007.

_____2. The Phase I proposal does not exceed $100,000.

DMEA SBIR 07.2 Topic Index

DMEA SBIR 07.2 Topic Descriptions

DMEA07-1 TITLE: High-Throughput Experimentation Physical Vapor Deposition (PVD) Chamber for Accelerated Microelectronics Materials Research and Development

TECHNOLOGY AREAS: Materials/Processes, Electronics

The technology within this topic is restricted under the International Traffic in Arms Regulation (ITAR), which controls the export and import of defense-related material and services. Offerors must disclose any proposed use of foreign nationals, their country of origin, and what tasks each would accomplish in the statement of work in accordance with section 3.5.b.(7) of the solicitation.

OBJECTIVE: Develop a PVD chamber capable of depositing multiple material conditions in isolated areas on a single silicon wafer, enabling multiple experimental data points to be accomplished rapidly on a single silicon wafer.

DESCRIPTION: The cost to maintain Moore's law is growing exponentially with every generation of semiconductor device. To support the ever-increasing demand for smaller, faster, lower-power, and lower-cost microelectronic semiconductor devices, tools enabling faster and lower-cost research and development are required. Current development tools are only capable of achieving one set of process parameters (i.e., test sites) per wafer. The goal of this effort is to determine the feasibility of developing a PVD chamber capable of placing 100 or more tests sites on a single wafer. The deposition process at each site will be independently controlled. This will enable incremental variations in semiconductor process parameters. If successful, this will result in orders of magnitude reduction in both time and cost for the microelectronic research and development efforts.

PHASE I: Develop a concept for the High-Throughput Experimentation PVD chamber capable of independent processing of 100 or more individual test sites per wafer. The test results for each independent site must correlate with full wafer processing.

PHASE II: Develop and demonstrate a prototype chamber and validate the concept developed in Phase I.

PHASE III: There may be opportunities for the further development of this concept for use in both military and commercial semiconductor fabrication activities. During a Phase III program, the contractor will refine the design of the chamber and apply the concept demonstrated in previous phases to specific semiconductor process problems.

DUAL USE COMMERCIALIZATION: The chamber will be applicable to both commercial and military semiconductor device research and development.

REFERENCES: 1) Tadatsugu, Minami, Mochizuki Yuu; and Miyata Toshihiro. "Combinatorial Deposition of EL Phosphor Thin Films by R.F. Magnetron Sputtering Using a Subdivided Powder Target." Thin Solid Films 494.1-2 (Jan 3, 2006): 33-37.
2) Gerein, Nathan J. and Joel A. Haber. "Physical Vapor Deposition Synthesis of Cu3BiS3 for Application in Thin Film Photovoltaics." MRS Proceedings 865 (Spring 2005): F5.36.
3) Hata, Seiichi, Ryusuke Yamauchi, Junpei Sakurai, and Akira Shimokohbe. "Combinatorial Arc Plasma Deposition of Thin Films." Japanese Journal of Applied Physics 45.4A (2006): 2708-2713.

KEYWORDS: Physical vapor deposition, semiconductors, semiconductor fabrication, semiconductor processing, microelectronics

DMEA07-2 TITLE: In-Line Characterization System for Advanced High K Dielectric / Metal Gate CMOS Transistor Stack for the Development of High Speed, Low Power Microelectronics

TECHNOLOGY AREAS: Materials/Processes, Electronics

The technology within this topic is restricted under the International Traffic in Arms Regulation (ITAR), which controls the export and import of defense-related material and services. Offerors must disclose any proposed use of foreign nationals, their country of origin, and what tasks each would accomplish in the statement of work in accordance with section 3.5.b.(7) of the solicitation.

OBJECTIVE: Develop a contactless, in-line system to electrically characterize advanced high-K dielectric / metal gate CMOS transistor stacks.

DESCRIPTION: The key metrics necessary to accelerate the development and integration of advanced gate stacks are primarily electrical (e.g. work function, leakage, etc.). In order to measure these parameters today, wafers must be processed through the first metal layer in order to form electrical contacts. This measurement delay slows down the learning rate which, in turn, impedes progress toward the effective integration of these high-performance structures. Using non-contact probes such as e-beams and specially-designed test structures will enable these electrical measurements to be made in-line, immediately after the gate stack formation. Moving these measurements in-line will accelerate learning and result in more effective and cost-efficient integration of these new structures.

PHASE I: Develop a concept for the characterization system; including definition of the inspection equipment and a preliminary design of the system, the test structures to be inspected, and the inspection methodology to achieve statistically valid results.

PHASE II: Build an engineering model of the system based on the concept and preliminary design developed during Phase I. Demonstrate the engineering model system and validate the test structures and sampling concepts.

PHASE III: There may be opportunities for the further development of this concept for use in both military and commercial semiconductor fabrication activities. During a Phase III program, the contractor will further develop the concept, and demonstrate it's application and utility in specific semiconductor fabrication lines.

DUAL USE COMMERCIALIZATION: The characterization system will be applicable for developing state of the art commercial devices as well as high performance, high reliability military devices.

REFERENCES: 1) Talbot, Christopher G., Richard Barnard, John Jamieson, Chiwoei W. Lo, Pierre Perez, and Andy Pindar. “Productive Application of Voltage Contrast for Detection of Optically Undetectable Defects.” Proceedings of SPIE 3677 (June 1999): 480-90. Rpt in Metrology, Inspection, and Process Control for Microlithography XIII. Ed. Bhanwar Singh.
2) Grella, Luca, Matthew Marcus, Gian Lorusso, and David L. Adler. “SEM voltage contrast simulations”. Proceedings of SPIE 3777 (November 1999): 133-41. Rpt. in Charged Particle Optics IV. Ed. Eric Munro.
3) Moreau, O., A. Kang, V. Mantovani, I. Mica, L. Avaro, C. Pastore, and G. Pavia. “Utilization of Electron Beam Inspection for Early Detection of Crystal Defects in Device Fabrication.” Advanced Semiconductor Manufacturing Conference (2005).

KEYWORDS: Microelectronics, test equipment, non-contact probes, e-beam probes

DMEA07-3 TITLE: Ultra Low-Power Miniaturized Flexible Radio Optimized for Long-Term Battery Operation

TECHNOLOGY AREAS: Sensors, Electronics

The technology within this topic is restricted under the International Traffic in Arms Regulation (ITAR), which controls the export and import of defense-related material and services. Offerors must disclose any proposed use of foreign nationals, their country of origin, and what tasks each would accomplish in the statement of work in accordance with section 3.5.b.(7) of the solicitation.

OBJECTIVE: Develop and demonstrate the design for a flexible, reconfigurable radio transceiver implemented on a microelectronic device that is suitable for long term operation (one year or more) on battery power.

DESCRIPTION: A flexible reconfigurable radio transceiver consists of a digital radio (or software radio) core and required oscillators, mixers, and amplifiers needed for specific applications. The digital radio core includes the transmitter exciter that modulates/encodes the transmitted signal by means of digital processing algorithms, converts the resultant data stream to an analog signal that can drive a power amplifier or mixer, and a digital receiver that performs an analog-to-digital conversion on the incoming signal or the signal from a mixer then demodulates/decodes the resultant digital data stream by use of signal processing algorithms. The frequency of operation of the digital radio core may be limited and on-chip frequency conversion may be required for operation at higher frequencies.

The digital radio may be easily reprogrammed to use different modulation methods. This makes it a useful building block for many different types of systems used by both military and commercial users.

An ultra-low power radio is meant to be powered by batteries over long periods of time (months or years) without replacement. This makes it useful in deployed sensor array systems with possible applications in ad-hoc networks.

The goal for power consumption for the receiver portion of the transceiver is 1 milliwatt or less in active receive mode during signal acquisition (listening) and 5 milliwatts or less when actively receiving a data stream of 100,000 bits per second or less, and 20 milliwatts or less while actively receiving a data stream of 100,000 to 2,000,000 bits per second. The goal for the entire radio during programmed sleep mode is less than 100 microwatts. The goal for the transmitter portion of the radio is zero power during any non-transmitting mode.

The goal for frequency coverage of the initial implementation of the radio is for configuration between 100 MHZ and 1,000 MHZ with a minimal number of external components and the ability to use an external LO to mix the RF signals up to 2.5 GHz. Frequency coverage of the radio after external component selection should be at least 10% of the minimum configured operating frequency.

The goal for on-chip transmitter power output is +20 dBm (100 milliwatts). Provision for controlling an external power amplifier and antenna switch should be made to allow arbitrarily high power operation.

A perfected ultra-low power flexible reconfigurable radio will enable timely fielding of task-specific radio transceivers, with the major development effort in software rather than hardware.

PHASE I: Research and develop a conceptual design that fulfills most or all of the goals above. Determine the feasibility of implementation on available semiconductor processes. Identify technical risks and prepare a risk mitigation plan.

PHASE II: Design, develop, and characterize a prototype microelectronic implementation of the transceiver based on the Phase I conceptual design.

PHASE III: There may be opportunities for the further development of this concept for use in both military and commercial activities. During a Phase III program, the contractor will further develop the concept, refine the design, or apply the technology to specific applications. In addition, it may be desirable to extend the frequency coverage to between 1 GHz and 2.5 GHz.

DUAL USE COMMERCIALIZATION: Military applications include data collector nodes for deployed sensor arrays, sensors, and other applications where very low power consumption combined with flexibility is desired. Commercial applications include battery powered communications, process control sensors, medical applications, and data collector nodes for sensor groups.

REFERENCES: 1) Ostman, Kim B., Sami T. Sipila, Ivan S. Uzunov, and Nikolay T. Tchamov. “Novel VCO Architecture Using Series Above-IC FBAR and Parallel LC Resonance.” IEEE Journal of Solid-State Circuits 41 (October 2006): 2248-2255.
2) Zhang, Frank, and Peter R. Kinget. “Design of Components and Circuits Underneath Integrated Conductors.” IEEE Journal of Solid-State Circuits 41 (October 2006): 2265-2271.

3) Shrestha, Rameswor, Eric A. M. Klumperink, Eisse Mensink, Gerard J. M. Wienk, and Bram Nauta. “A Polyphase Multipath Technique for Software-Defined Radio Transmitters.” IEEE Journal of Solid-State Circuits 41 (December 2006): 2681-2692.
4) Cook, Ben W., Axel Berny, Alyosha Molnar, Steven Lanzisera, and Kristofer S. J. Pister. “Low-Power 2.4-GHz Transceiver With Passive RX Front-End and 400-mV Supply.” IEEE Journal of Solid-State Circuits 41 (December 2006): 2757-2766.
5) Lueftner, Thomas, Joerg Berthold, Christian Pacha, Georg Georgakos, Guillaume Sauzon, Olaf Hoemke, Jurij Beshenar, Peter Mahrla, Knut Just, Peter Hober, Stephan Henzler, Doris Schmitt-Landsiedel, Andre Yakovleff, Axel Klein, Richard J. Knight, Pramod Acharya, Andre Bonnardot, Steffen Buch, and Mattias Sauer. “A 90-nm CMOS Low-Power GSM/EDGE Multimedia-Enhanced Baseband Processor With 380-MHz ARM926 Core and Mixed-Signal Extensions.” IEEE Journal of Solid-State Circuits 42 (January 2007): 134-144.

KEYWORDS: Microelectronics, RF, radio, low-power